A Class D Amplifier Using MOSFETs with Reduced Minority Carrier Lifetime*

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Design techniques are presented for a 0.5-MHz class D amplifier using specially processed MOSFETs with ultrafast intrinsic diode recovery characteristics. Design problems and solutions are presented for the power, filter, and modulator stages. Problems and results are discussed using error correction by loop feedback from the output filter and supply feedforward to the modulator stage. An overview is included of power supply issues, including a lightweight power-factor-corrected quasi-resonant switching power supply.

1 POWER-STAGE BASIC TOPOLOGIES

The topology chosen for this switching amplifier is the "classic" buck pulse-width-modulated (PWM) switch in a full bridge configuration. Alternatives considered include the half-bridge and a four-quadrant Cuk converter [1]. The basic Cuk converter can be thought of as a combination buck/boost converter using capacitors as an intermediate energy transfer element. If properly designed, it can achieve near zero ripple currents, making it relatively easy to achieve low electromagnetic interference (EMI). Furthermore, a four-quadrant converter may be configured with all drive circuits referred to ground. The Cuk converter is not without some drawbacks, though. The individual converter blocks have a fairly nonlinear gain characteristic, which is balanced to a degree in the four-quadrant converter. The characteristics of the charge transfer capacitor have a significant effect on circuit balance and overall distortion [2]. Furthermore, the additional series inductors required to meet the "zero output ripple" condition create another pole in the transfer function, which tends to peak the output response at a frequency well below the output corner frequency. This may be damped by an *RC* damper of the Cuk capacitors, but it requires capacitors twice the value of the Cuk capacitors. Output impedance is relatively high, rendering the Cuk converter fairly load sensitive. Furthermore, this design requires *p*- and *n*-type devices for grounded operation, rendering high-power converters impractical due to the 3:1 resistance handicap of *p*-channel MOSFETs.

1.1 Basic Characteristics of Buck PWM Converter

The half-bridge and full-bridge buck converters present their own set of problems, but offer some benefits in return. The inherent transfer function is quite linear, and the number of reactive energy storage elements is minimized. Achieving low output voltage ripple with a single *LC* stage is problematic at switching frequencies that result in good efficiency. As for all buck converters, input current ripple is fairly high and has a high harmonic content. To achieve low losses at high power, all *n*-channel devices should be used, and this necessitates isolated, "floating" drivers with considerable precision and speed. Although some converters in principle allow simple ground-referred drive circuits with direct connection to analog control circuits, experience and the reports of other researchers [2] show that it is impractical to mix fast digital and drive circuits with "clean" analog circuits on a common ground. The author's experience is that analog control and feedback circuits must be isolated to the greatest degree possible from the driver and switching power blocks; this prin-

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ciple drove a number of design decisions. Under these ground rules, the development of a "clean" buck converter is not at as much at disadvantage as might be thought. Furthermore, its inherently linear transfer function and low output impedance are very desirable qualities. The overall topology developed is outlined in Fig. 1, which includes the basic control loop, modulator, and output-stage signal paths. Note that the modulator circuit uses switched current sources to create a high-frequency triangle wave. The square-wave oscillator is derived from the divided output of a crystal oscillator at 5 MHz. The triangle amplitude is a function of the current source amplitude, which includes a fixed reference component and a component derived from the power-supply rail voltage. By this means the modulator-stage gain is corrected by feedforward so that the variations in output level, which would occur because of supply-voltage variations, are suppressed. This includes effects such as variations in power supply voltage, which occur as a result of high output signal levels.

1.2 Bridge Configurations

Several factors were considered when choosing between a half-bridge and a full-bridge switch configuration. Component cost and count will at first glance appear lower for the half-bridge circuit. However, for a given power level, the full bridge allows the use of MOSFETs with one-half the drain-source breakdown-voltage rating ($V_{DS(BRR)}$). Though the full-bridge circuit has two switches in series with the load, the drain-source on-resistance ($R_{DS(ON)}$) of 200-V MOSFETs is less than one-half that of the 400-V types with comparable chip area. As an example, the BUZ250 with a 20-mm^2 chip is rated at 250 V, 0.24 Ω, and 17 A, while the BUZ331, with a 25-mm^2 chip, is rated at 500 V, 0.8 Ω, and 8.0 A. For the same number of MOSFETs, conduction losses can be lower with the full bridge. The lower voltage MOSFETs also have considerably lower Q_{rr}, contributing to lower switching losses should the intrinsic diode carry current. Other issues are noise and distortion. For the full-bridge circuit, even-order distortion products will cancel. Furthermore, the high-frequency switching loop may be confined to the power supply rails, while in the half-bridge circuit the power loop includes the ground circuit in the path, not just as a reference point. The opposing current paths in the bridge circuit may be used to advantage to reduce the effective inductance in the high-frequency current path by overlaying opposing conductor traces [3]. The area

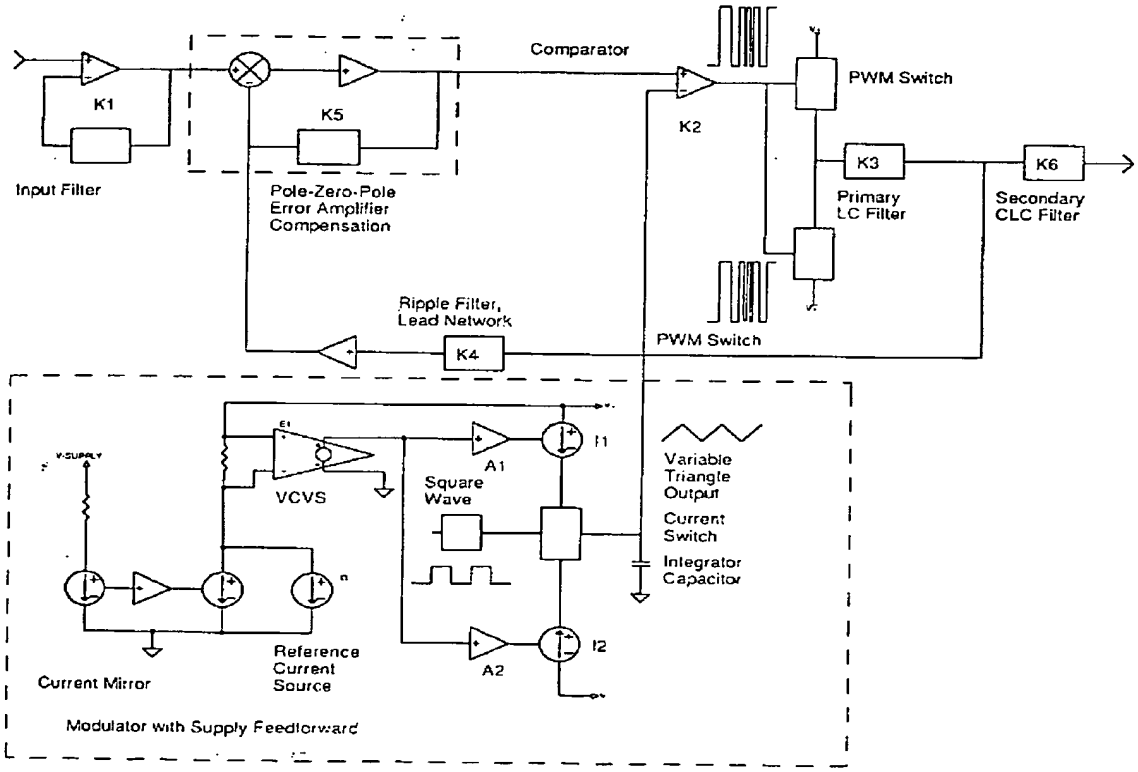


Fig. 1. Class D amplifier using supply feedforward.

of the magnetic field can be confined to a very small area, minimizing inductance and radiated energy.

1.3 Switching Transistors and Any Parallel Diodes

In a buck switching amplifier the output filter presents an inductive load to the switching stage. In some bridge applications, such as motor drives, the inductive load current is handled by antiparallel energy recovery diodes connected between the switch load and the power supply rails. As Atwood noted [4], [5], switching between active device conduction and recovery diode conduction introduces a "crossover notch" step function in the output waveform. His (patented) approach to solving this problem uses a tapped inductor to provide a voltage offset for the recovery diode. Additional diode clamps are provided for adjustable inductors inserted in series with each switching leg. These are necessary to prevent avalanched or dv/dt failures in the MOSFETs, which occur if the parasitic bipolar structure (Fig. 2) is turned on [6]. In combination, these efforts reduce distortion and improve reliability, but the tapped inductor configuration puts considerable constraints on the inductor design and must be optimized for a specific line voltage.

The intrinsic diode of conventional power MOSFETs has a carrier lifetime and charge storage that are controlled by doping characteristics of the silicon and by the thickness of the n region. As voltage ratings rise, so does the required thickness of the n region, and with it the diode recovery time. Typical 500-V MOSFETs show recovery times of 500 ns from 8-A forward current at 100-A/μs di/dt. During this recovery phase the peak I_{DRM} may become very high. This makes turn-on of the parasitic bipolar likely, particularly at elevated junction temperatures. Near the end of the recovery phase occurs a critical interval, when high dv/dt is applied (Fig. 3). If the MOSFET parasitic bipolar has been turned on, it will fail because of the safe operating area (SOA) limitations of the parasitic bipolar device, whose $V_{CE(SUS)}$ is approximately one-half the $V_{DS(BRR)}$ rating of the MOSFET.

It is essential to prevent body diode conduction in conventional MOSFETs, because diode recovery losses become a major contributor to switching losses, and because of this dv/dt failure mode. This usually requires the use of antiparallel diodes, Schottky diodes in series with the MOSFETs, which contribute to increased conduction losses. The only other solution is to improve the MOSFET.

Carrier lifetime can be affected by processes such as proton irradiation or heavy-metal implanting. These processes create minor imperfections in the silicon crystalline lattice, which facilitate carrier recombination. Siemens has found a platinum implant process to be the most effective and yielding excellent stability of characteristics with repeated thermal cycling. The BUZ250 is a 250-V fast-recovery epitaxial diode field effect transistor (FREDFET) with improved diode characteristics [7]. It exhibits a typical recovery time of 85 ns from 17-A forward diode current (Fig. 4). This compares very favorably with ultrafast diodes, which are typically rated for 50-ns recovery from a forward current of 1 A. As the test current is increased, stored charge and recovery time increase. Furthermore, this new MOSFET has very high immunity to bipolar turn-on, giving it high dv/dt capability in this mode. This makes it suitable for use in applications where inductive recovery current may flow in the body diode of the MOSFET.

1.4 Design Verification Using SPICE Simulations

Much of the design exploration and initial verification for this switching amplifier was done using SPICE simulations of the power and control circuit. A typical problem with this approach is the lack of complex device models, including usable power MOSFET models. The

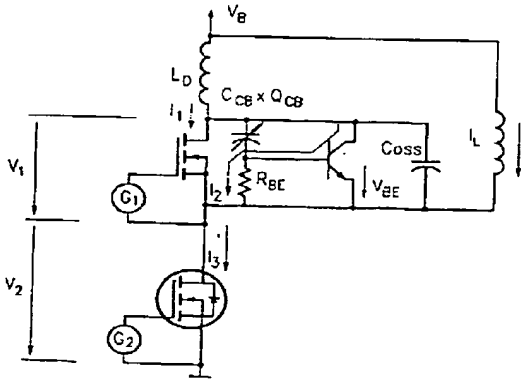


Fig. 2. Simplified equivalent bridge circuit of SIPMOS FET, depicting voltages and conduction paths during commutation and reverse recovery of inductive load.

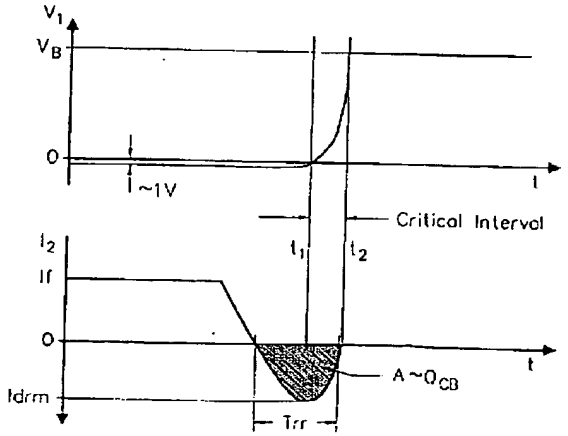


Fig. 3. Typical current and voltage characteristics of intrinsic body diode during commutation.

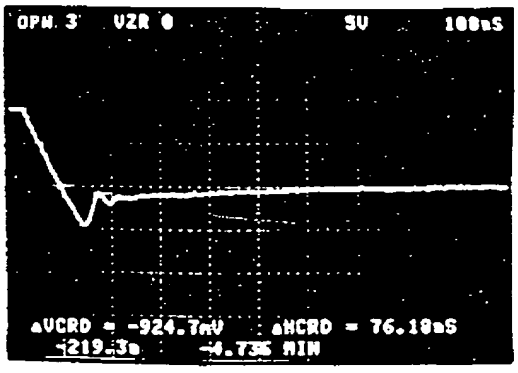
built-in models for SPICE were developed for simulating IC circuits. In the case of MOSFETs, there are considerable differences in device structures and electrical characteristics between lateral MOS transistors used in IC structures and vertical power MOSFETs [8]. In the case of the lateral MOS transistor, the gate overlays a horizontal current path between source and drain. Switching characteristics do not change a great deal with variation in V_{DS}. The gate-to-drain capacitance is very nonlinear for vertical MOSFETs, as it includes a depletion capacitance element. In addition, there is no provision in the SPICE MOS model for the intrinsic diode formed by drain to the p well.

A SPICE subcircuit model has been developed (Fig. 5) using SPICE MOS, JFET, and diode models to form a structure equivalent to the vertical MOSFET [9]. This model uses polynomial voltage-controlled voltage source (VCVS) with fixed capacitor to model the nonlinear gate-to-drain capacitance, producing results valid for both ac and transient simulations [19].

Given the finite nature of computing resources, it is necessary to use a hierarchical approach to preparing simulations of complex circuits [10]. For this reason, a detailed examination of driver circuit issues should take place at a different level than an examination of overall topology issues or control circuits. For this development effort, simulations of varying detail were done at the driver circuit level (Fig. 6), at the complete power switch bridge circuit (Fig. 8), analyzing the output filter (Fig. 14), and for the complete control loop (Fig. 19).

1.5 Driver Circuits

Preparation of the driver circuit simulations required developing macro models of the comparator and driver chips that were under evaluation (Fig. 6). The driver simulation was used to predict peak gate drive currents and rise and fall times as a function of layout parasitics and component values. MOSFETs have very high C_{GD} at low V_{DS}, and hence a long T_D off. The driver was designed to swing ±7 V, speeding up turnoff considerably when compared with drive circuits that only sink to the source potential. Though there is a slight $R_{DS(ON)}$ penalty from not using a 10-V drive, the overall drive power is reduced by 50%, making it a worthwhile tradeoff. Since floating driver circuits are required, isolated low-power auxiliary supplies power the driver ICs and opto couplers. A miniature dual-bobbin EP-10 transformer with 12 pF of interwinding capacitance is used at 100 kHz for powering each of the driver circuits. The schematic of the driver stage developed is shown in Fig. 7. A "power good" comparator (not shown) is also used to gate the drive signals and provide undervoltage lockout, as well as shutdown in the event of driver overloads. High-speed, high-common-mode rejection ratio opto couplers are used to couple the drive signals. The opto couplers have a longer time delay off than on (due to hole carrier recombination in the light-emitting diode). To compensate for this delay, an additional opto coupler stage is used at the comparator outputs in inverted phase to add on a variable delay, thus preventing cross conduction.



ig. 4. Reverse recovery time measurement of BUZ250 REDFET.

1.6 Evaluation of Bridge Switching Circuit Using a MOSFET Models

The complete bridge topology used is shown in Fig. 8. It is similar to a previously reported circuit [3] using MOSFETs directly without Schottky blocking diodes. However, it uses coupled inductors instead of individual di/dt inductors in each half-bridge, as in [11], with fast-recovery clamp diodes directly connected to the opposite rail voltage. A coupled inductor model was developed based on Graetz's nonlinear inductor model [12]. The SPICE coupled inductor model has problems with transient simulations in circuits involving recirculating currents. Even using macro models, this is a relatively complex circuit to simulate, but it can be run in a few hours on a 386-based PC.

Figs. 9–12 show simulation results for the final version of the bridge, running for 50 μs with a 20-kHz sine wave "signal" input. The printing interval was set for 25 ns, and the minimum time step interval for 5 ns. Fig. 9 shows the 20-kHz signal input and the 500-kHz triangle wave with both phases of comparator output. Fig. 10 shows gate-voltage waveforms and drain-voltage rise and fall times for one of the switch blocks. Fig. 11 shows the voltage at one of the half-bridge outputs and the current through the switch leg monitored by a zero-voltage voltage source, ISRC1. The voltage

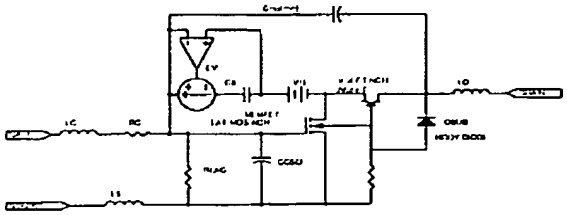


Fig. 5. MOSFET subcircuit model with POLY fit for C_{GD}.

from the *LC* filter output is shown in Fig. 12.

Evaluation of this circuit showed that minimizing inductance in the power supply leads and the diode clamps was critical to developing clean waveforms and minimizing voltage overshoots on the drain circuits of the MOSFETs. Circuit inductance is one of the few areas in which there are choices available that can make a key difference in overall behavior. In older high-power circuits, with clock frequencies in the audible range, conventional bus bar or heavy-gauge stranded wire is most commonly used for connections. Any interconnect should be considered as an air core inductor and evaluated as such for its effect on circuit performance.

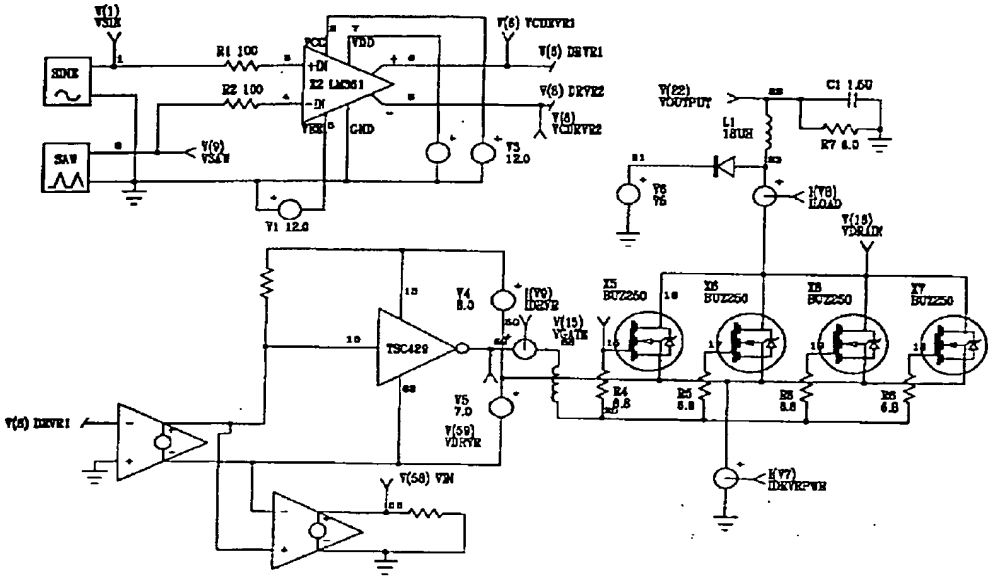


Fig. 6. SPICE driver simulation circuit with macro models.

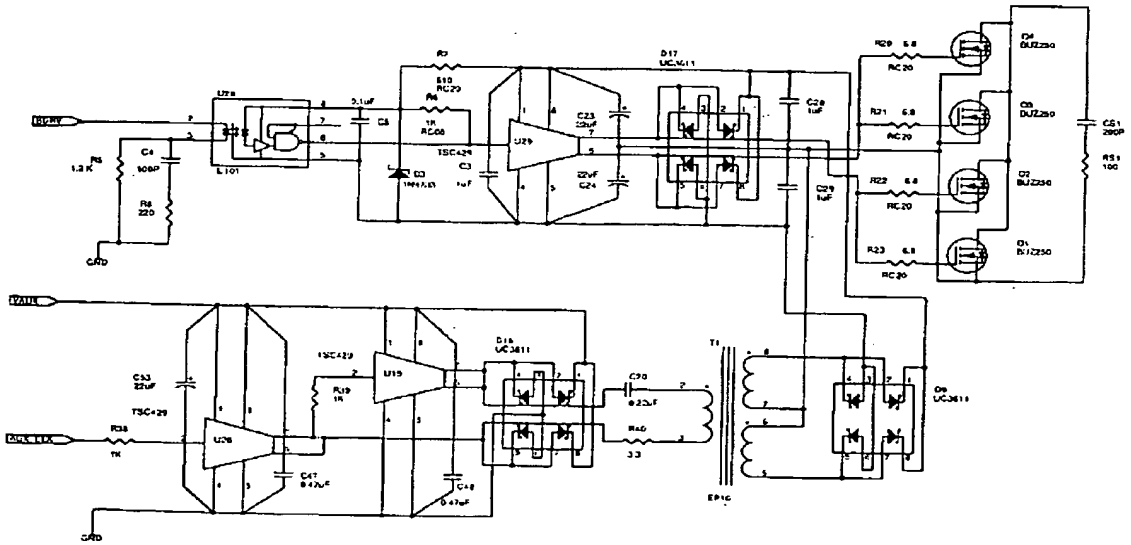


Fig. 7. Isolated driver supply and gate drive schematic.

For the case of inductance where the energy is stored in an air gap,

$$L = \mu_0 N^2 A / \mathcal{L}$$

where μ_0 is the permeability of free space, A is the current through N turns enclosed by the magnetic path $\mathcal{L}$. Taken a little further, one can define the inductance of a wire in free space from its length and diameter,

$$L = 0.002 W_l \left[\log \left(\frac{4W_l}{W_d} \right) - 1 + \frac{\mu}{4} \right]$$

where W_l is the conductor length and W_d the conductor diameter, both in centimeters, and μ is the permeability.

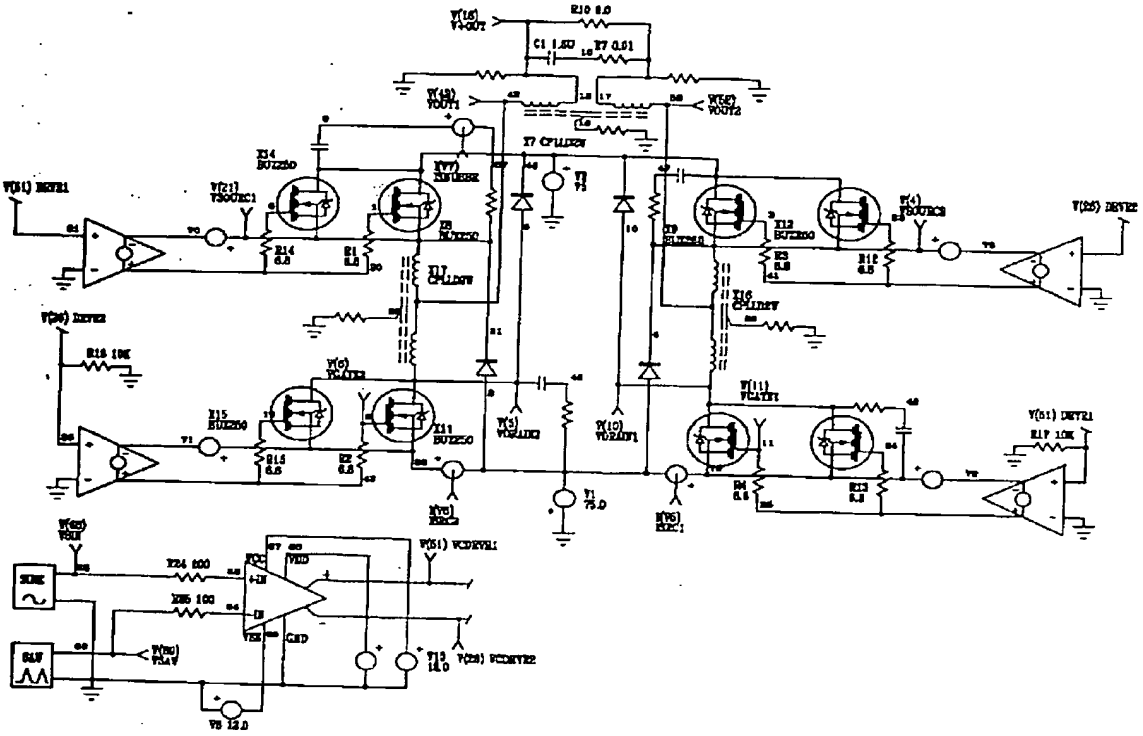
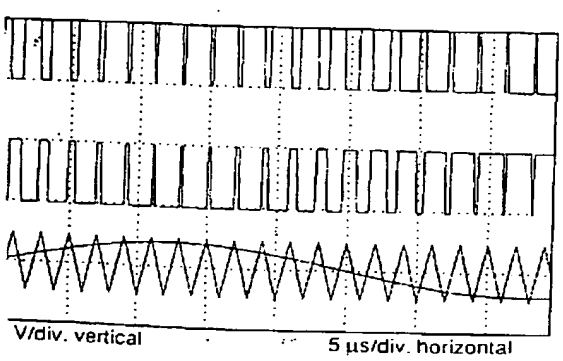


Fig. 8. Bridge switch with di/dt limiting coupled inductors.



g. 9. 500-kHz ramp; 20-kHz sine and comparator outputs.

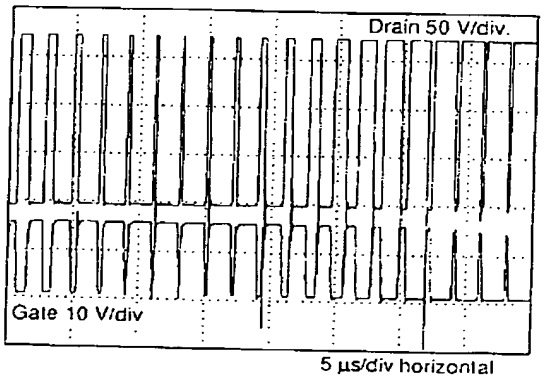


Fig. 10. Gate and drain simulation waveforms.

For a given length of a conductor having a given diameter, it does not appear from this equation that there is much we can do. Any circuit includes both a send and a return current path. As one brings two conductors carrying opposing currents close together, the magnetic field becomes concentrated between them, reducing the area of the field and the inductance.

Using a close relative of the previous equation, we can calculate the expected inductance from one more parameter, the conductor spacing,

$$L = 0.004 W_l \left[\log \left(\frac{2W_p}{W_d} \right) + \frac{\mu}{4} - \frac{W_p}{W_l} \right]$$

where W_p is the parallel conductor spacing in centimeters.

This function is plotted in Fig. 13, showing that dramatic reductions in inductance are possible if opposing current paths are overlayed in high-power high-frequency circuits. This principle was applied to the full bridge, resulting in a power switch layout with 16 transistors and 8 diodes in a space approximately 4 by 4 in (100 by 100 mm).

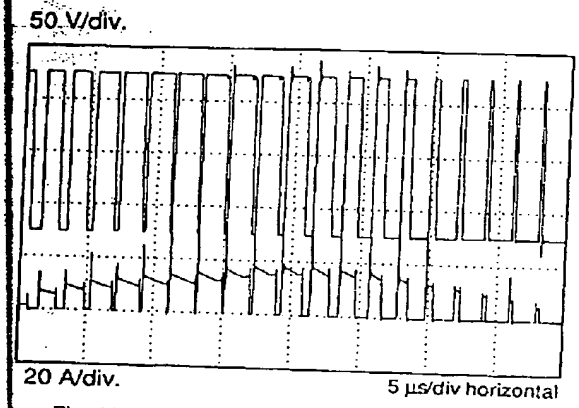


Fig. 11. Output voltage and ISRC$_1$ monitor points.

2 SIGNAL-PATH TOPOLOGY

2.1 Evaluating the Output Filter with Realistic Component Models

The output filter is another design problem where component characteristics and parasitic elements have a significant role in affecting the results expected at frequencies of hundreds of kilohertz. The small-signal model for the power stage and filter is shown in Fig. 14. The output filter is a combination of LC low-pass filter at 25 kHz and a resonant bandstop filter at 500

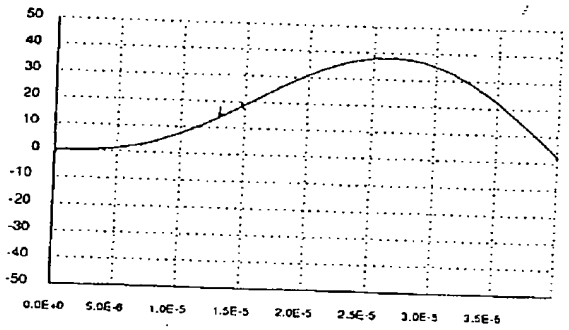


Fig. 12. LC filter output simulation.

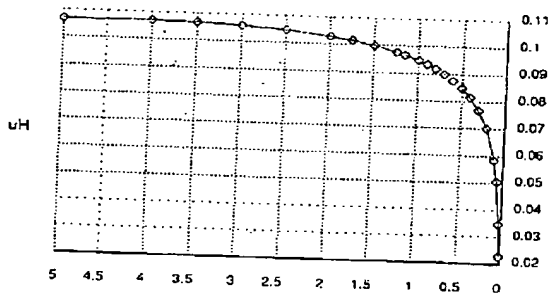


Fig. 13. Inductance (μH) as a function of conductor spacing (cm).

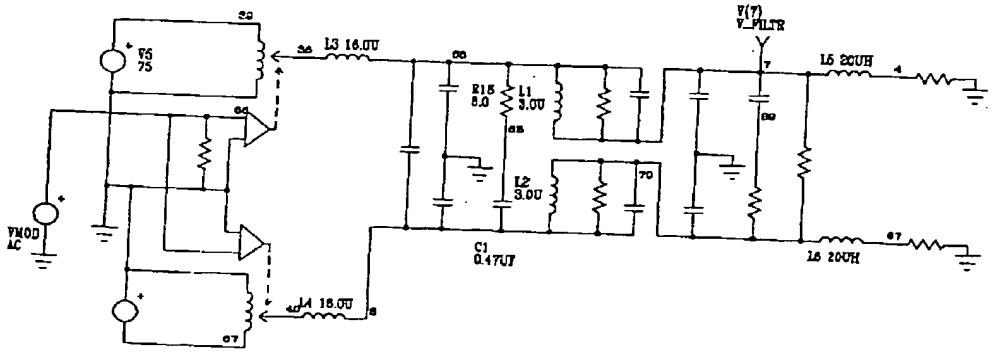


Fig. 14. Circuit for small-signal analysis of output filter.

kHz, which adds an additional low-pass element at 100 kHz [3]. The ideal filter is calculated using standard methods, and may be analyzed using standard S functions or an admittance matrix. The result of a SPICE simulation using "ideal" components and a resistive load for the calculated filter circuit is shown in Fig. 15. Predicted attenuation at the clock frequency of 500 kHz is approximately 100 dB. If a load having inductive and resistive characteristics is substituted, the Q of the filter changes, resulting in some peaking at the resonant frequencies (Fig. 16).

An "ideal" filter will not be possible to build, so it is desirable to explore the characteristics of one modeled with the nonideal resistance and inductance of capacitors. With this modification, the filter characteristics can be more realistically assessed, as in Fig. 17, which includes models for fairly high-quality capacitors. Fig. 18 shows the final filter characteristics with damping resistors for the CLC section, and RC networks for impedance stabilization at high frequencies.

The complete small-signal model is given in Fig. 19. A four-pole input filter is used with a corner frequency of 25 kHz. X37 is a balanced differential feedback amplifier with lead compensation to compensate for one of the poles of the output filter; this is necessary to allow closed loop stability around an LC filter. This model includes a ripple filter formed by R54, R56, C37, and C35, whose purpose is to reduce the spike ripple seen by the error amplifier. Feedback is taken after the first LC filter section, but before the additional phase shift of the bandstop filter. The error amplifier uses a pole–zero–pole scheme common to switching power supplies to control loop gain. The previously described output filter and small-signal power-stage model completes the loop. Fig. 20 shows the results plotted for open-loop gain of the feedback and error amplifiers. The phase lead peaks at 100 kHz, where loop crossover is desired. Note that to achieve adequate lead compensation at these high frequencies requires using operational amplifiers whose bandwidth extends to several megahertz without degradation. Fig. 21 displays the net loop gain, showing loop crossover just below 100 kHz, with a phase margin of about 65°. The net loop characteristic is quite close to the ideal 6-dB per octave rolloff. The predicted closed-loop response is shown in Fig. 22, as well as the error amplifier level versus frequency with the loop closed. This indicates that the input filter characteristic is fairly well matched to the output stage bandwidth, as little peaking of error amplifier levels occurs.

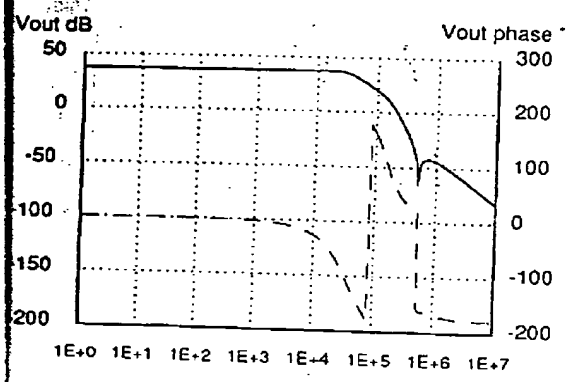


Fig. 15. "Ideal" filter with resistive load.

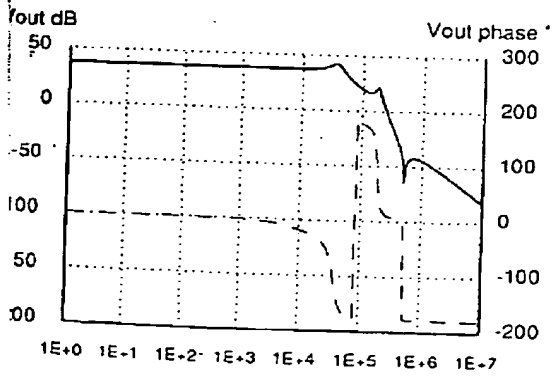


Fig. 16. "Ideal" filter with resistive/inductive load.

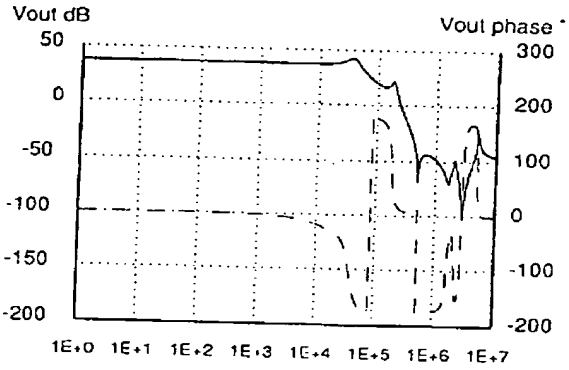


Fig. 17. "Real" filter with resistive/inductive load.

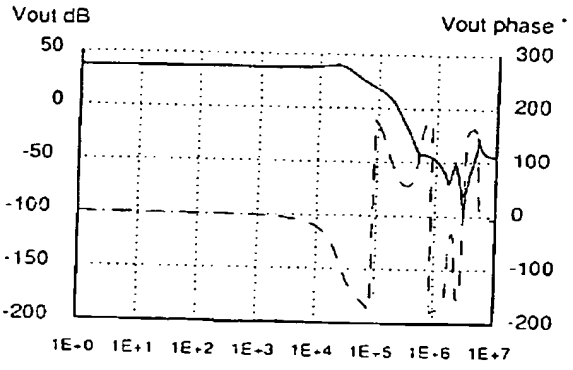


Fig. 18. "Real" filter with damping networks.

3 OUTPUT WAVEFORMS

Actual output waveforms, recorded with a Tektronix 7D20 waveform digitizer, are shown in Figs. 23–26. The output from one of the half-bridge sections is shown in Fig. 23 at approximately 150 V peak to peak. Correlation with the simulation results is quite good. High-level, high-frequency output is shown open loop in Fig. 24, displaying the high degree of basic linearity in the power stage. The next graph, Fig. 25, illustrates low-level linearity with 12.5-kHz output at 500 mV/div. Output noise voltage is shown in Fig. 26, displaying a base-

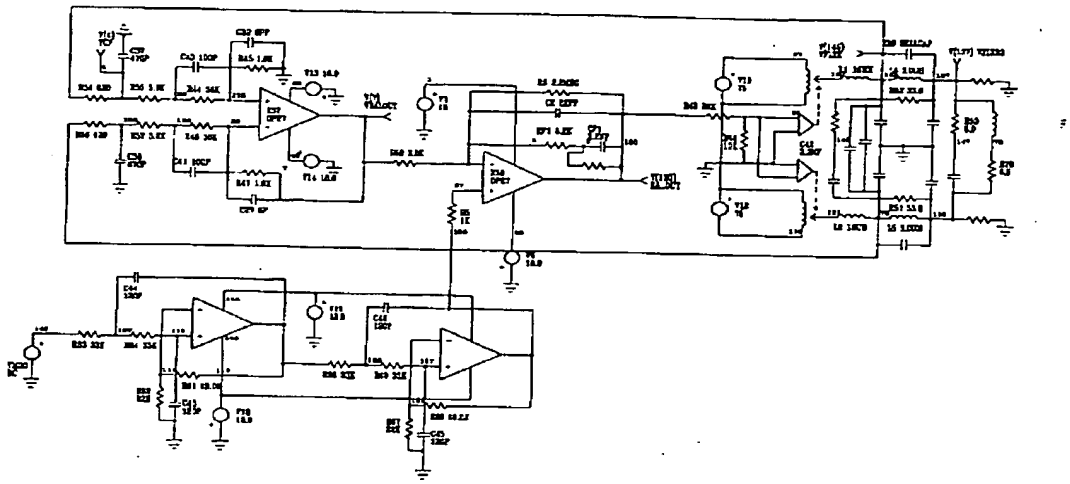


Fig. 19. Complete small-signal model for simulation.

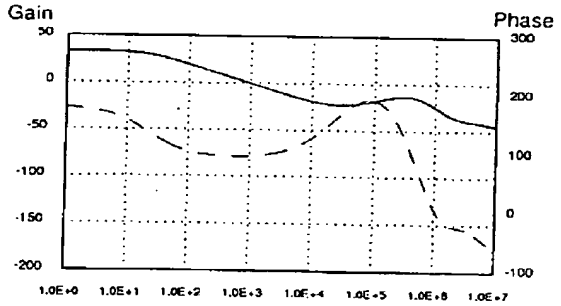


Fig. 20. Feedback and error amplifier simulation of gain and phase.

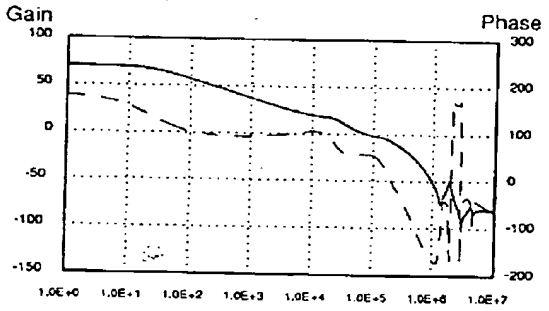


Fig. 21. Simulation of compensated open-loop gain and phase.

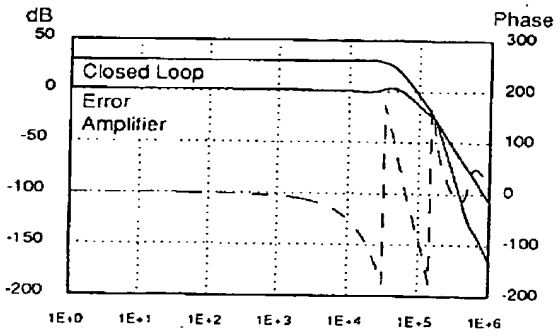


Fig. 22. Predicted closed-loop response.

band ripple of 50 mV peak to peak, with switching spikes somewhat greater than 100 mV. Most of the spike ripple can be eliminated by further optimization of the filter layout and an additional VHF filter block, as might be implemented using bulkhead feedthrough capacitors.

4 OVERVIEW OF HIGH-EFFICIENCY POWER-FACTOR-CORRECTED POWER SUPPLY

4.1 Power Factor—The Problem with Capacitor Input Power Supplies

The majority of power amplifiers produced use 50/60-Hz transformers and capacitor input filter rectification. As power levels rise, so do the weight and expense. Furthermore, though these supplies are quite simple electrically, they are not as "clean" on the power line as most of their users would expect. Like capacitor input switching power supplies, the input current flows in relatively narrow spikes, resulting in high harmonic content and high peak currents in proportion to the true power consumed. This is illustrated in concept in Fig. 27, which shows the ac voltage waveform, the current conduction when the ac wave exceeds the filter droop voltage, and the input filter voltage ripple. Typical capacitor input circuits exhibit a power factor of 0.7, which, in simple terms, means that a circuit designed for 1000-W delivery into a resistive load can only deliver 700 W into this load.

In power supply applications such as airborn electronics, the power factor has long been a concern and specified parameter. Of late it is receiving more attention for industrial and consumer equipment, particularly in Europe, where new IEC standards classify non-power-factor-corrected equipment with waveforms such as Fig. 27 as class D equipment, with attendant penalties and restrictions.

One method gaining in popularity to solve this problem is the use of a switching converter as a current preregulator to program the current draw to follow the line voltage [13]. Typically a boost or flyback converter is used as a preregulator to charge a 360-V bus that powers a secondary converter, which provides isolation and load regulation. A low value of high-frequency ripple, which is easily filtered, is superimposed on the 50/60-Hz low-frequency current waveform, as shown in Fig. 28. The cost of two converters is offset by several factors. Because the secondary regulator sees a relatively stabilized voltage, the secondary converter

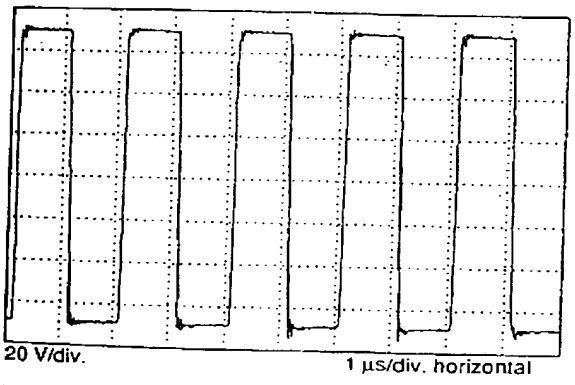


Fig. 23. 500-kHz-waveform voltage feeding output filter.

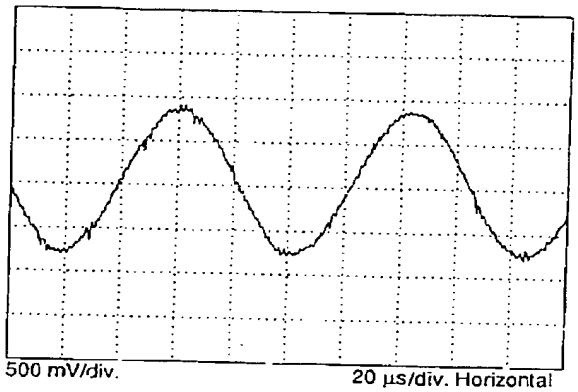


Fig. 25. Low-level 12.5-kHz-output open loop.

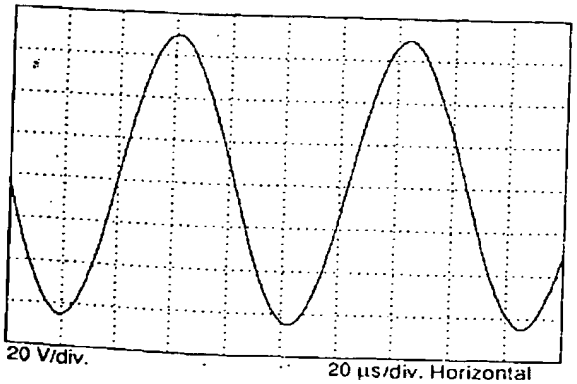


Fig. 24. 12.5-kHz-output open loop.

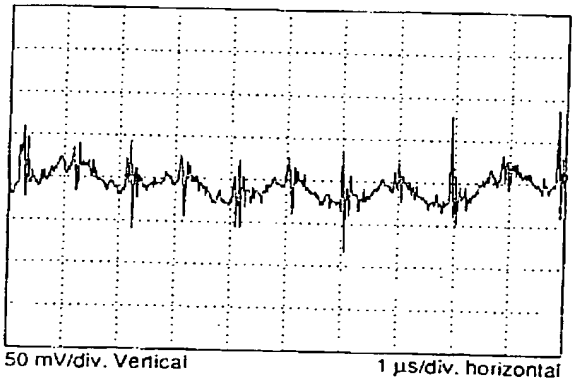


Fig. 26. Output ripple voltage across balanced outputs.

components can be sized more ideally. The ripple currents are considerably reduced in the filter capacitors by this technique, saving cost in the capacitors and semiconductor switches. Last, but probably not least, this circuit can provide automatic line-voltage adaptation, working from 90 to 260 V ac without any taps or switches.

4.2 Low-Noise ZCS-QRC Main Converter

For the secondary converter, objectives in an amplifier power supply must include very low ripple, inherently good load regulation, and high efficiency. For an amplifier application, high power density, or small size, is of secondary importance. Although a conventional switching power supply may achieve some of these goals, newer topologies show that improvements can be made, particularly in regard to EMI and noise.

Resonant and quasi-resonant converters have been developed in many topologies to achieve high power density through minimum magnetics volume and very high switching frequencies, often in the megahertz range. By using reactive components, including reactive parasitics of switching devices or transformers, a nonsquare current or voltage waveform is achieved, decreasing the stress and losses for switching transitions when compared with conventional PWM "square-wave" switching power supplies. Whereas early PWM switching power supplies operated at a few tens of kilohertz, resonant supplies have been developed at frequencies as high as tens of megahertz [14]–[18]. If high power density is not the goal, lower frequency ranges may be used with transistors such as IGBTs [17], [18] to achieve good efficiency and very reasonable di/dt's (and low noise) with switching rates in the 100-kHz region. Fig. 29 shows the basic power switch circuit for one type of quasi-resonant power supply, a zero-current-switching parallel quasi-resonant converter. This type of supply switches the voltage across the transistors at nearly zero current (Fig. 30), resulting in low switching losses, and very low switching stress on output components, as the voltage output waveforms are haversines. Almost any kind of PWM supply may be built as an equivalent resonant circuit. The parallel quasi-resonant circuit is most similar to the buck PWM

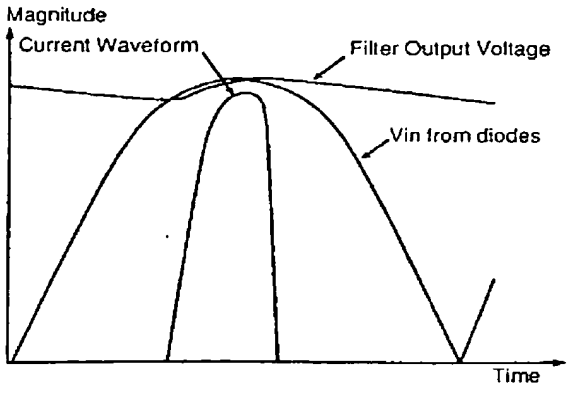


Fig. 27. Capacitor input rectifier waveforms.

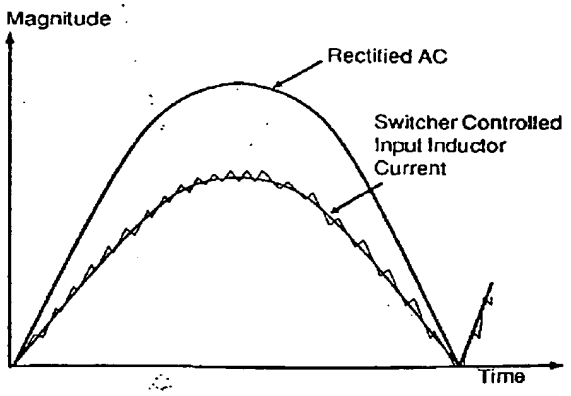


Fig. 28. Power-factor converter input current.

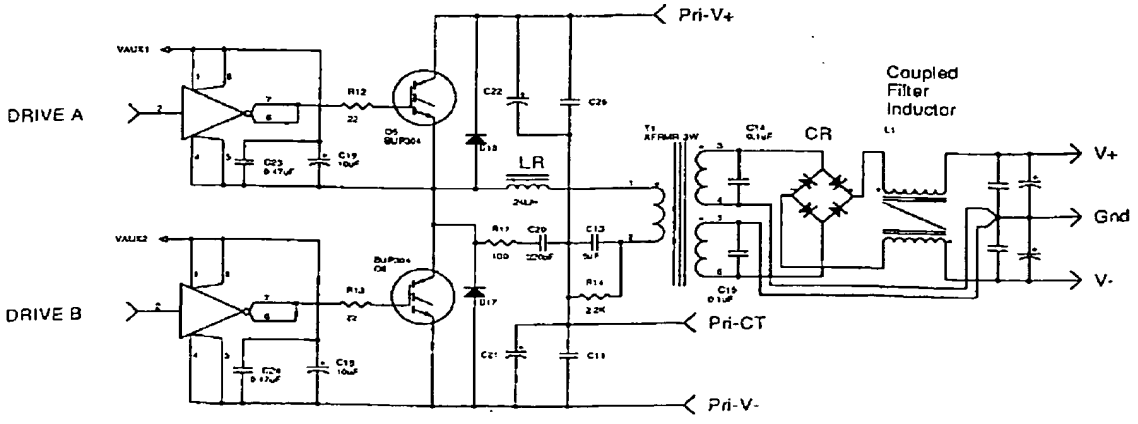


Fig. 29. Basic circuit for half-bridge ZCS-QRC.

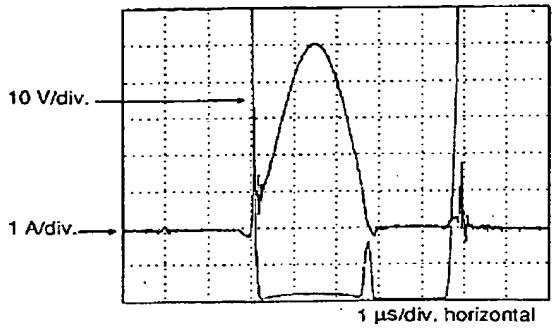


Fig. 30. Typical transistor voltage and current waveforms.

converter and, like the buck equivalent circuits, has low output impedance and inherently good load regulation.

Although "unconventional" power supplies (that is, not 50/60-Hz transformer isolated with capacitor input filters) are uncommon in audio, the convergence of component, design, and power quality issues may change that picture.

SUMMARY

A new power MOSFET has been developed using heavy metal doping, which is well suited to developing a switching amplifier. A bridge circuit is described which supports fast switching and has a good waveform shape at 500 kHz. SPICE modeling is shown to be a useful tool for design verification of many aspects of the circuit operation, including driver circuits, bridge switch, output filter, and control loops.

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Jon Mark Hancock was born in 1951 in Providence, RI. Though formally educated in music and a working musician for 10 years, his interest in music electronics lead to his joining Intersound in the late 1970s to develop instrument preamplifiers, equalizers, and amplifiers for live performance. When that company was sold, he joined Tecnetics, Inc., Boulder, CO, a manufacturer of Mil-type power supplies. There worked in a QA